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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Larry Eugene Mosley
Title: HIGH PERFORMANCE CAPACITOR
Attorney Docket No.: 884.209US1

PATENT APPLICATION TRANSMITTAL

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X Utility Patent Application under 37 CFR § 1.53(b) comprising:
- X Specification (13 pgs, including claims numbered 1 through 29 and a 1 page Abstract).
- X Formal Drawing(s) (6 sheets).
- X Unsigned Combined Declaration and Power of Attorney (3 pgs).

X Information Disclosure Statement (1 pgs), Form 1449 (1 pgs), and copies of cited references (3).

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UNITED STATES PATENT APPLICATION

HIGH PERFORMANCE CAPACITOR

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HIGH PERFORMANCE CAPACITOR

Field

The present invention relates to capacitors, and more particularly to capacitors having a high capacitance, low inductance, and low resistance.

Background

Voltage levels on a die exhibit a droop when there is a sudden increase in demand for power on the die. This voltage droop on the die increases the switching time of the transistors on the die, which degrades the performance of the system fabricated on the die. To decrease the voltage droop during power surges, discrete decoupling capacitors are mounted adjacent to the die and connected to the conductors that provide power to the die. For a processor die, the die is mounted on a substrate, and a ring of capacitors, usually ten to fifteen two microfarad capacitors, are mounted on the substrate along the periphery of the die. These capacitors are coupled to the power supply connections at the die through lands formed on the substrate. Problems with this decoupling solution and the capacitors used to implement this solution are long standing, well known, and interrelated.

One problem with this decoupling solution is that a large number of external decoupling capacitors are required to control the voltage droop on a die. Mounting a large number of external decoupling capacitors wastes substrate real estate and reduces the die packing density on the substrate. In addition, surface area on the substrate is reserved for handling and mounting the discrete capacitors, and this reserved area is unavailable for mounting other information processing dies.

A second problem with this decoupling solution relates to the long leads needed to connect the capacitors to the power supply connections sites on the die. Power supply connection sites are usually scattered across a die. In general, it is desirable to run short leads from a power supply plane in a substrate to the power supply sites on the die. Unfortunately, with the decoupling capacitors located near the periphery of the die, long leads must be run to the power supply connection sites scattered across the die. The long

leads increase the inductance and resistance of the decoupling capacitors, which tends to increase the voltage droop in response to a power surge. The long leads used to connect a die to a decoupling capacitor limit the high frequency performance of the decoupling capacitor.

A third problem is that capacitors having a large capacitance value typically have a large inherent inductance and resistance. This inherent inductance and resistance causes a large voltage droop at the die.

One solution to these problems is to fabricate a large number of capacitors on the die for decoupling the power supply connections on the die. Unfortunately, capacitors already take up a large amount of real estate on a die for a typical integrated circuit, and fabricating more capacitors on a die reduces the area available for information processing circuits.

For these and other reasons there is a need for the present invention.

Summary

A capacitor comprises a plurality of conductive layers embedded in a dielectric. A plurality of vias couple at least two of the plurality of conductive layers to a plurality of connection sites.

Brief Description of the Drawings

Figure 1A is an illustration of a cross-sectional side view of some embodiments of a capacitor of the present invention.

Figure 1B is an illustration of a top view of a capacitor showing one embodiment of a controlled collapse chip connection pattern.

Figure 2 is an illustration of a cross-sectional view of some embodiments of a system including a capacitor coupled to a plurality of substrates.

Figure 3 is an illustration of a cross-sectional view of one embodiment of a system including a die and a capacitor coupled to a substrate.

Figure 4 is an illustration of a cross-sectional view of some embodiments of a system including capacitor coupled to a plurality of electronic dies.

Figure 5 is an illustration of a cross-sectional view of some embodiments of a system including a capacitor coupled to a dielectric substrate and electrically coupled to a die.

Detailed Description

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the claims.

The present invention provides a high capacitance, low profile capacitor having a low inductance and a low resistance and a system for mounting the capacitor close to a die. To fabricate a high capacitance low profile capacitor, a plurality of thin screen printed dielectric sheets are stacked to form the capacitor. To reduce the inductance and resistance in the capacitor leads, a large number of vias are coupled to the conductive layers printed on the stacked dielectric sheets. Finally, to control the length of the leads that couple the capacitor to a die, the vias at the surface of the capacitor are fabricated to couple to a substrate using controlled collapse chip connection technology. Alternatively, to control the length of the leads that couple the capacitor to a die, the capacitor is mounted on a laminated layer and vias are laser drilled and plated to provide the electrical connection to the capacitor.

Figure 1A is an illustration of a cross-sectional side view of some embodiments of capacitor 100 of the present invention. Capacitor 100, in one embodiment, is a multilayered capacitor including a first plurality of conductive layers 103 and 104 interlaced with a second plurality of conductive layers 105 and 106. Increasing the number of conductive layers in capacitor 100 increases the capacitance. In one

embodiment, capacitor 100 has about 50 conductive layers and a capacitance of between about 20 microfarads and 30 about microfarads. Conductive layers 103-106 are fabricated from a conductive material. For example, in one embodiment, conductive layers 103-106 are fabricated from platinum. Alternatively, conductive layers 103-106 are fabricated from palladium. In still another alternate embodiment, conductive layers 103-106 are fabricated from tungsten. Conductive layers 103-106 are embedded in dielectric 113. Conductive layers 103 and 104 are coupled together by vias 115 and 116, and conductive layers 105 and 106 are coupled together by vias 117 and 118. In one embodiment, vias 115-118 are plated through holes that terminate on outer surfaces 127 and 130 in a plurality of connection sites, such as controlled collapse chip connection (C4) sites 133. A large number of C4 sites decreases the resistance and the inductance of capacitor 100, which improves the performance of capacitor 100 as a decoupling capacitor. In one embodiment, capacitor 100 has about 4000 C4 sites. Controlled collapse chip connection sites 133 are not limited to being fabricated on a single surface. In one embodiment, C4 sites 133 are fabricated on outer surfaces 127 and 130. Providing C4 sites on a plurality of surfaces increases the number of electronic dies or devices that can be coupled to capacitor 100. Coupling structures for capacitor 100 are not limited to C4 structures. In one embodiment, vias 115-118 terminate on outer surfaces 127 and 130 in pads suitable for coupling to a substrate, an electronic device, or a die.

In one embodiment, capacitor 100 has a thickness 136 of between about .5 millimeter and about 1 millimeter, a top surface area of about 1 cm^2, and a capacitance of between about 20 microfarads and about 30 microfarads. A capacitance of between about 20 microfarads and about 30 microfarads makes capacitor 100 suitable for use in decoupling high frequencies that appear on power supply lines in complex digital systems, such as microprocessors. A thickness 136 of between about .5 millimeter and about 1 millimeter makes capacitor 100 suitable for packaging with communication devices, such as cell phones, that are packaged in a small volume.

Figure 1B is an illustration of a top view of capacitor 100 of Figure 1A showing one embodiment of a pattern of controlled collapse chip connection sites. In one embodiment, the controlled collapse connection sites 133 have a pitch of between about

100 microns and about 500 microns. A pitch of between about 100 and about 500 microns reduces the inductance and resistance in the connections. In one embodiment, C4 site 139 is coupled to a high voltage level, and C4 sites 142, 145, 148, and 151 are coupled to a low voltage level. Each high voltage level C4 site is surrounded by four low voltage level sites. This pattern of power distribution in the C4 sites reduces the inductance and resistance in capacitor 100, which improves the high frequency performance of capacitor 100.

For one embodiment of a method for fabricating capacitor 100, a plurality of dielectric sheets are screen printed with a tungsten paste or other suitable suspension of tungsten and stacked. The dielectric sheets are fabricated from barium titanate and have a thickness of between about 5 microns and about 7 microns. The tungsten paste forms the conductive layers 103-106 of capacitor 100. To add strength to the stack, slightly thicker dielectric sheets are used to form the top and bottom layers of the stack. Via holes are formed in the stack to couple conductive layers 103-106 to controlled collapse chip connection sites 133. Processes suitable for use in forming the via holes include mechanical drilling, laser drilling, and etching. The via holes are filled with a metal slurry, which, in one embodiment, is formed from tungsten. To further increase the rigidity of the stack, the stack is co-fired at about 1500 degrees centigrade and diced into individual capacitors.

Figure 2 is an illustration of a cross-sectional view of some embodiments of system 200 for coupling capacitor 100 to substrates 206 and 209. Substrates 206 and 209, in one embodiment, are fabricated from a ceramic. Alternatively, substrate 206 is a die, such as a silicon die, and substrate 209 is fabricated from a ceramic. In one embodiment, capacitor 100 is coupled to substrates 206 and 209 through controlled collapse chip connections (C4) 210 and 211. C4 connection sites 133 on the surfaces 127 and 130 of capacitor 100 are coupled through solder balls 215 to connection sites 218 and substrates 206 and 209. First and second metallization layers 221 and 224 in substrate 206 and first and second metallization layers 227 and 230 in substrate 209 can be coupled to devices mounted on substrates 206 and 209, thereby coupling capacitor 100 to the devices. The capability to couple capacitor 100 to a plurality of substrates permits

increased packing densities for complex electronic devices fabricated in connection with substrates 206 and 209. For example, several microprocessors can be packaged on substrates 206 and 209, and the power supply connections for the several microprocessors can be decoupled by capacitor 100. By reducing the number of discrete decoupling capacitor packages that are required to decouple the several microprocessors, the reliability of the system 200 is increased.

Figure 3 is an illustration of a cross-sectional view of one embodiment of system 300 for coupling die 303 to capacitor 100 through common substrate 306. In one embodiment, die 303 includes an electronic device, such as a processor, a communication system, or an application specific integrated circuit. Die 303 is coupled to a first surface of substrate 306 by controlled collapse chip connection (C4) 309. Capacitor 100 is coupled to a second surface of substrate 306 by controlled collapse chip connection 312. Conductive vias 315 in substrate 306 couple capacitor 100 to die 303. In one embodiment, substrate 306 is fabricated from a ceramic material. Alternatively, substrate 306 is fabricated from an organic material. Preferably, substrate 306 is thin, which permits a short coupling distance between capacitor 100 and die 303. In one embodiment, substrate 306 has a thickness 318 of less than about 1 millimeter. A short coupling distance reduces the inductance and resistance in the circuit in which capacitor 100 is connected.

Figure 4 is an illustration of a cross-sectional view of some embodiments of system 400 including capacitor 100 coupled to electronic dies 403 and 406. Substrate 409 provides a foundation for mounting die 403 and capacitor 100. In addition, substrate 409 couples die 403 to capacitor 100 through vias 412. Similarly, substrate 415 provides a foundation for mounting die 406 and capacitor 100, and couples die 406 to capacitor 100 through vias 422. Connections, such as controlled collapse chip connections 418-421 couple die 403, die 406 and capacitor 100 to substrates 409 and 415. For substrate 409 having a thickness 423 of less than about 1 millimeter and substrate 415 having a thickness 424 of less than about 1 millimeter, the resistance and inductance of capacitor 100 and vias 412 and 422 is low. So, decoupling power supply connections at die 403 and 406 is improved by packaging dies 403, 406 and capacitor 100 as described above.

Figure 5 is an illustration of a cross-sectional view of some embodiments of a system 500 including capacitor 503 coupled to substrate 506 and electrically coupled by vias 512 and controlled collapse chip connection 512 to die 515. Capacitor 503 is coupled to power supply connections on die 515 to decouple the power supply connections at the die. Capacitor 503 is protected from the environment by molding 518. In one embodiment, substrate 506 is formed from a low K dielectric and has a thickness 521 of between about .05 millimeters and about .1 millimeters. A dielectric thickness of between about .05 millimeter and .1 millimeter allows system 500 to be fabricated with shorter capacitor leads than the capacitor leads in system 400. As described above, a system having short leads between capacitor 503 and die 515 results in a capacitor having a low inductance and a low resistance, which improves the performance of the decoupling circuit.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A capacitor comprising:

a plurality of conductive layers embedded in a dielectric; and

a plurality of vias coupling at least two of the plurality of conductive layers to a plurality of connection sites.

2. The capacitor of claim 1, wherein the capacitor has a thickness of between about .5 millimeter and about 1 millimeter.

3. The capacitor of claim 2, wherein the capacitor has a capacitance of between about 20 and about 30 microfarads.

4. The capacitor of claim 1, wherein the plurality of controlled collapse chip connection sites have a pitch of between about 100 and about 500 microns.

5. The capacitor of claim 1, wherein the plurality of vias are plated through holes.

6. A capacitor comprising:

a plurality of first conductive layers;

a plurality of second conductive layers interlaced with the plurality of first conductive layers;

a number of surfaces having a plurality of connection sites operable for coupling the capacitor to a substrate using a controlled collapse chip connection (C4); and

a plurality of vias coupling the plurality of first conductive layers and the plurality of second conductive layers to at least two of the plurality of connection sites.

7. The capacitor of claim 6, wherein each of the plurality of first conductive layers is fabricated from a tungsten paste.

8. The capacitor of claim 6, wherein the number of surfaces is two.

9. A capacitor comprising:

a multilayered capacitor having a number of outer surfaces; and

a number of pads located on at least two of the number of outer surfaces wherein at least two of the number of pads are capable of being coupled to a substrate using a solder bump.

10. The capacitor of claim 9, wherein the multilayered capacitor includes a number of parallel conductive layers and the number of pads are coupled to the number of parallel conductive layers through vias.

11. The capacitor of claim 10, wherein the number of conductive layers is greater than about 50.

12. The capacitor of claim 11, wherein the number of pads is greater than about 4000.

13. A system comprising:

a die including an electronic system;

a capacitor located less than about .1 millimeter from the die and coupled to the die, the capacitor is capable of decoupling a power supply connection at the die without additional capacitors located external to the die; and

a dielectric layer located between the capacitor and the die.

14. The system of claim 13, wherein the dielectric layer has a thickness of between about .05 millimeters and about .1 millimeters.

15. A system comprising:

a first die;

a second die; and

a capacitor having a first surface having a controlled collapse chip connection coupled to the first die and a second surface having a controlled collapse chip connection coupled to the second die.

16. The system of claim 15, wherein the first die includes a processor and the second die includes a communication system.

17. A system comprising:

a substrate having a surface; and

a capacitor having a plurality of vias coupled to a plurality of conductive layers in the capacitor, the capacitor is coupled to the surface at a plurality of connection sites.

18. A system comprising:

a substrate having a first surface and a second surface;

a die coupled to the first surface; and

a capacitor having a plurality of vias coupled to a plurality of conductive layers in the capacitor, the capacitor is coupled to the second surface by a controlled collapse chip connection and the capacitor is electrically coupled to the die through the substrate.

19. The system of claim 18, wherein the die includes a processor.

20. The system of claim 19, wherein the die has a die surface and the capacitor has a capacitor surface and the capacitor surface is located less than about .1 millimeter from the die surface.

21. A system comprising:

a processor requiring at least 5 watts of power to be operable; and

a single multilayered single package capacitor coupled to the processor and capable of decoupling a power supply from the processor.

22. The system of claim 21, wherein the single multilayered single package capacitor is capable of being mounted on a substrate by a plurality of solder bumps.

23. The system of claim 22, wherein the single multilayered capacitor is capable of being mounted on a substrate using a controlled collapse chip connection.

24. A method comprising:
forming a stack of a plurality of screen printed dielectric sheets;
forming a plurality of via holes in the stack;
filling at least two of the plurality of via holes with a metal slurry; and
co-firing the stack to form a capacitor.

25. The method of claim 24, further comprising:
coupling the stack to a substrate using a controlled collapse chip connection.

26. The method of claim 24, further comprising:
coupling a die to the substrate and to the capacitor.

27. A method comprising:
forming a capacitor having a plurality of conductive layers and a surface; and
forming a pattern of pads on the surface, at least one pad in the pattern of pads is capable of being coupled to at least one of the plurality of conductive layers and capable of being coupled to a substrate using a solder bump attachment.

28. The method of claim 27, further comprising:
coupling the capacitor to a ceramic substrate using a solder bump attachment.

29. A method comprising:
selecting a substrate having a controlled collapse chip connection capability; and

mounting a multilayered capacitor on the substrate using the controlled collapse chip connection capability.

Abstract

A capacitor includes a controlled collapse chip connection system coupled by vias to a plurality of conductive layers embedded in a dielectric. The capacitor and a die can each be mounted on opposite surfaces of a substrate using a controlled collapse chip connection. The controlled collapse chip connection provides a large number of leads for coupling to the conductive layers of the capacitor. The large number of leads reduce the inductance in the connection. For a thin substrate, the length of the conductive material connecting the capacitor to the die is short, and the inductance and resistance of the conductive material is low. A system comprising two dies can be fabricated in a small volume using a plurality of substrates and a single controlled collapse chip connection compatible capacitor for decoupling the two dies.

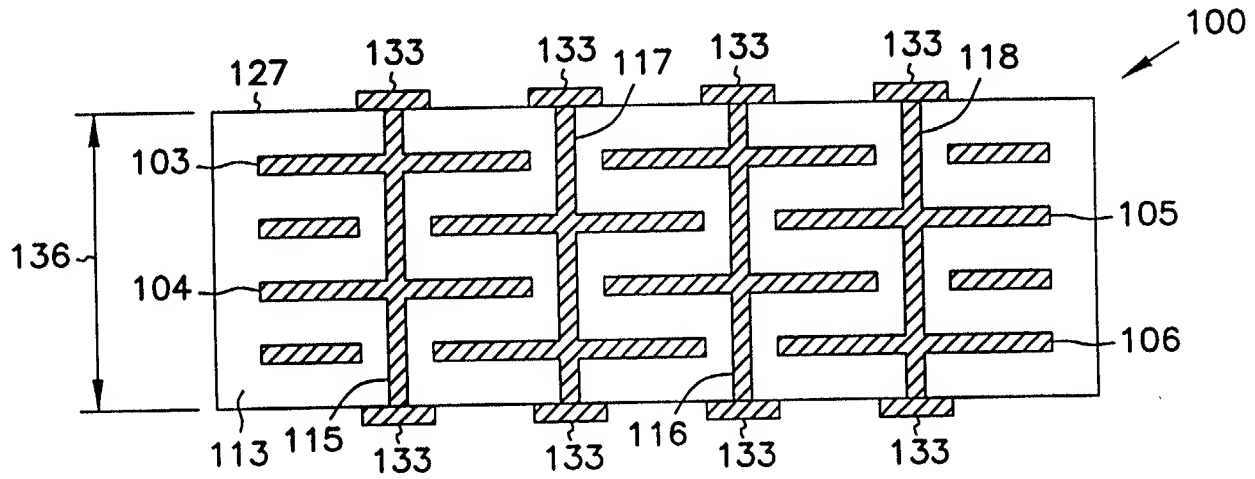

Figure 1A

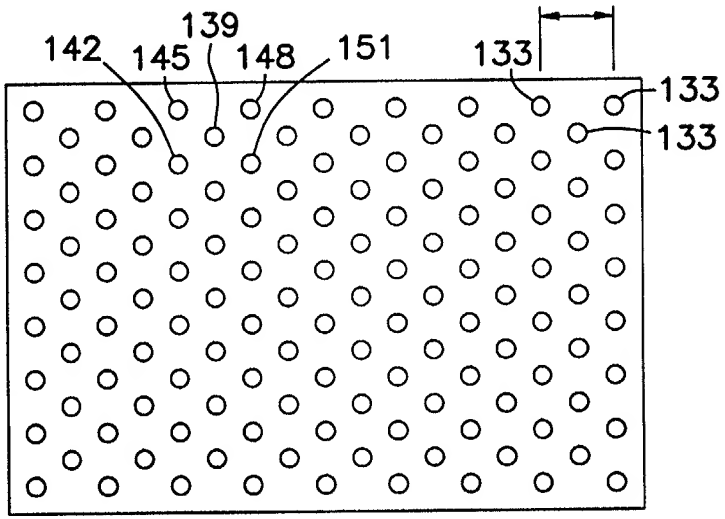

Figure 1B

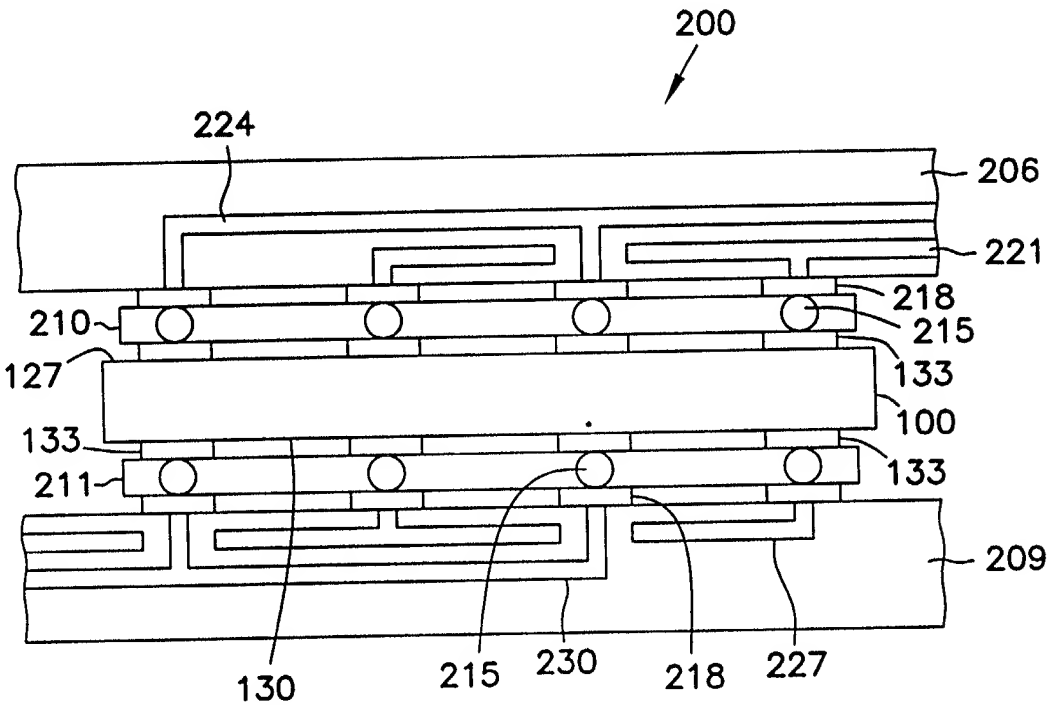
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Figure 2

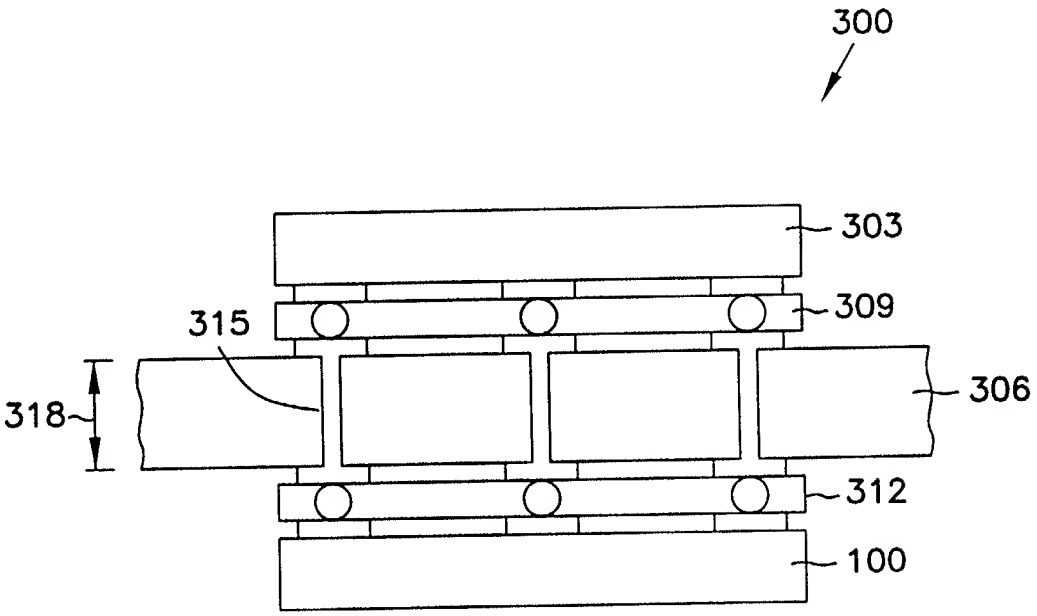

Figure 3

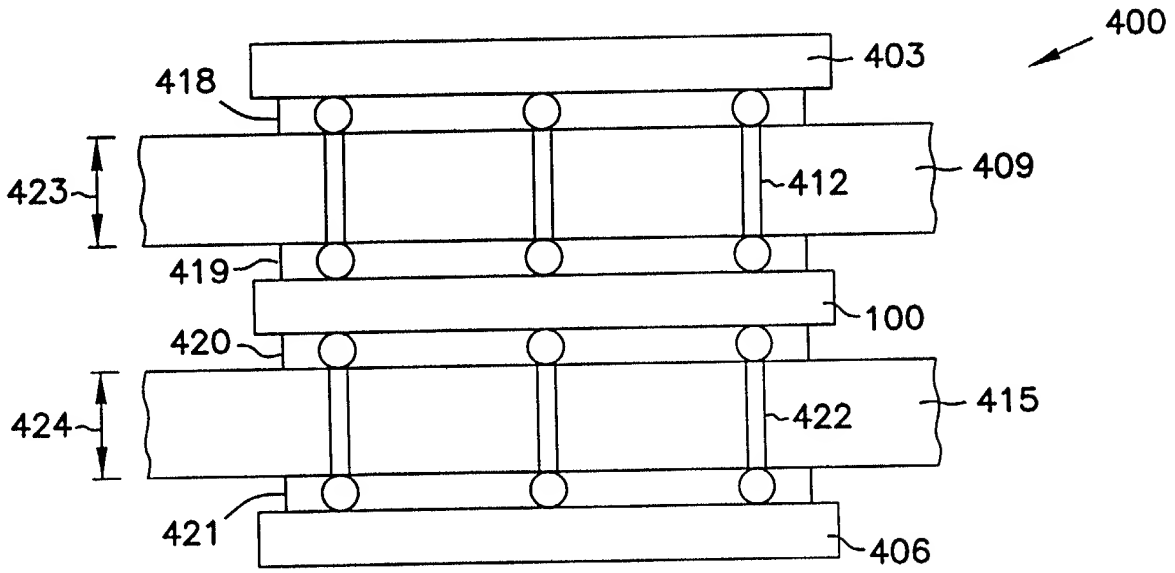

Figure 4

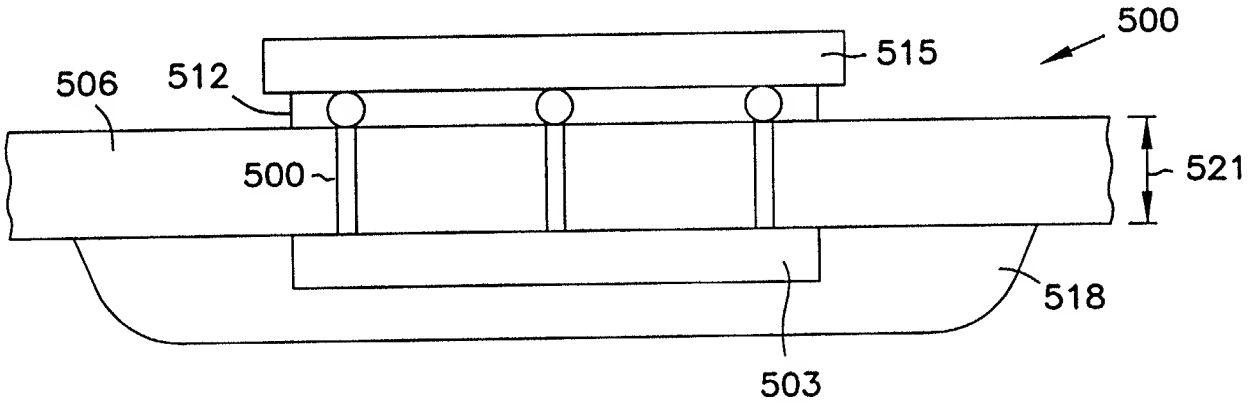

Figure 5

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **HIGH PERFORMANCE CAPACITOR**.

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 C.F.R. § 1.56 (attached hereto). I also acknowledge my duty to disclose all information known to be material to patentability which became available between a filing date of a prior application and the national or PCT international filing date in the event this is a Continuation-In-Part application in accordance with 37 C.F.R. §1.63(e).

I hereby claim foreign priority benefits under 35 U.S.C. §119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 120 or 365(c) of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

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I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

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Black, David W.	Reg. No. 42,331	Klima-Silberg, Catherine I	Reg No. 40,052	Parker, J Kevin	Reg No 33,024
Brennan, Leoniede M	Reg. No. 35,832	Kluth, Daniel J	Reg. No 32,146	Peacock, Gregg A	Reg. No 45,001
Brennan, Thomas F	Reg No. 35,075	Lacy, Rodney L	Reg No 41,136	Perdok, Monique M	Reg No. 42,989
Brooks, Edward J., III	Reg No 40,925	Leffert, Thomas W.	Reg. No 40,697	Polglaze, Daniel J	Reg No 39,801
Chu, Dinh C.P.	Reg No 41,676	Lemaire, Charles A	Reg No 36,198	Prout, William F	Reg. No. 33,995
Clark, Barbara J.	Reg No 38,107	Litman, Mark A	Reg No. 26,390	Schumm, Sherry W	Reg. No 39,422
Dahl, John M.	Reg No 44,639	Lundberg, Steven W	Reg. No. 30,568	Schwegman, Micheal L.	Reg No. 25,816
Drake, Eduardo E	Reg No 40,594	Mack, Lisa K	Reg No. 42,825	Slifer, Russell D	Reg. No 39,838
Eliseeva, Maria M	Reg No. 43,328	Maki, Peter C	Reg No. 42,832	Smith, Michael G	Reg No P-45,368
Embretson, Janet E.	Reg. No 39,665	Malen, Peter L.	Reg No 44,894	Steffey, Charles E	Reg. No. 25,179
Fogg, David N.	Reg. No 35,138	Mates, Robert E	Reg. No. 35,271	Terry, Kathleen R	Reg No 31,884
Fordenbacher, Paul J	Reg No 42.546	McCrackin, Ann M	Reg. No. 42,858	Viksnins, Ann S	Reg No 37,748
Forrest, Bradley A	Reg. No. 30,837	Nama, Kash	Reg No 44,255	Woessner, Warren D	Reg No 30,440
Harris, Robert J.	Reg No. 37,346				

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Please direct all correspondence in this case to **Schwegman, Lundberg, Woessner & Kluth, P.A.** at the address indicated below:

P.O. Box 2938, Minneapolis, MN 55402
Telephone No. (612)373-6900

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Sunnyvale, CA 94089

Signature: _____ Date: _____
Larry Eugene Mosley

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.